

1 3. The integrated circuit package of claim 1 comprising a plastic
2 encapsulant which encapsulates the silicon die and the transition medium, the plastic
3 encapsulant having a coefficient of thermal expansion between approximately
4 $7 \times 10^{-6}/^{\circ}\text{C}$ and $15 \times 10^{-6}/^{\circ}\text{C}$.

1 4. The integrated circuit package of claim 1 wherein the transition
2 medium comprises a mold compound material, a BT resin compound, a FR-4 compound,
3 or a FR-5 resin compound.

1 5. The integrated circuit package of claim 1 wherein the transition
2 medium has a coefficient of thermal expansion between approximately $7 \times 10^{-6}/^{\circ}\text{C}$ and 17
3 $\times 10^{-6}/^{\circ}\text{C}$.

1 6. The integrated circuit package of claim 1 wherein the presence of
2 the transition medium reduces stress and fracture damage to the silicon die.

1 7. The integrated circuit package of claim 1 wherein a thickness of
2 the metallized polymer layer and a thickness of the plastic encapsulant define a package
3 thickness, wherein the silicon die is disposed near the middle of the package thickness.

1 8. The integrated circuit package of claim 7 wherein the package
2 thickness is approximately 0.060 inches or less.

1 9. The integrated circuit package of claim 5 wherein the silicon die
2 thickness is less than approximately 6 mils.

1 10. The integrated circuit package of claim 1 wherein the silicon die is
2 coupled to the transition medium through an adhesive.

1 11. The integrated circuit package of claim 1 wherein a coefficient of
2 thermal expansion for the adhesive is approximately $58 \times 10^{-6}/^{\circ}\text{C}$.

1 12. The integrated circuit package of claim 1 wherein the integrated
2 circuit metallized polymer layer is a tape carrier having a dielectric layer and a conductive
3 layer.

1 13. The integrated circuit package of claim 12 comprising solder balls
2 mounted to the second side of the metallized polymer layer, the solder balls electrically
3 contacting an etched circuit in a conductive layer of the tape carrier.

1 14. The integrated circuit package of claim 13 wherein the solder balls
2 electrically connect the integrated circuit package to a printed circuit board.

1 15. The integrated circuit package of claim 14 wherein the solder balls
2 are arranged in a grid fashion underneath the position for the silicon die.

1 16. The integrated circuit package of claim 1 wherein the cross
2 sectional area of the silicon die is substantially less than or equal to the cross sectional
3 area of the rigid transition medium.

1 17. The integrated circuit package of claim 1 wherein the cross
2 sectional area of the silicon die is larger than the cross sectional area of the transition
3 medium.

1 18. The integrated circuit package of claim 1 wherein the package is a
2 BGA package.

1 19. The integrated circuit package of claim 1 wherein a volume of the
2 silicon die is less than the volume of the rigid transition medium.

1 20. An integrated circuit package comprising:
2 a metallized polymer layer defining a first thickness;
3 a transition medium coupled to the metallized polymer layer;
4 a die coupled to the transition medium; and
5 a mold cap encapsulating the transition medium and the die, the mold cap
6 defining a second thickness, wherein the first thickness and second thickness define a
7 package thickness, wherein the die is disposed near the middle of the package thickness.

1 21. The integrated circuit package of claim 20 wherein the mold cap
2 has a coefficient of thermal expansion similar to a coefficient of thermal expansion of the
3 transition medium.

1 22. The integrated circuit package of claim 20 wherein the die is
2 mounted to the transition medium with a layer of adhesive.

1 23. The integrated circuit package of claim 20 wherein the transition
2 medium comprises a mold cap material, a second layer of adhesive, an elastomer, a BT
3 resin compound, a FR-4 compound, or a FR-5 resin compound.

1 24. The integrated circuit package of claim 20 wherein the metallized
2 polymer layer is a tape carrier.

1 25. An integrated circuit package comprising:
2 a tape carrier;
3 a first adhesive layer disposed on the tape carrier, the first adhesive layer
4 having a coefficient of thermal expansion;
5 a transition medium having a first surface and a second surface, wherein
6 the first surface of the transition medium engages the first adhesive layer, the transition
7 medium having a coefficient of thermal expansion;
8 a second adhesive layer disposed on the second surface of the transition
9 medium, the second layer of adhesive having a coefficient of thermal expansion; and
10 a die disposed on the second adhesive layer; and
11 a mold cap encapsulating the first adhesive layer, the transition medium,
12 the second adhesive layer and the die, wherein the mold cap and tape carrier define a
13 package thickness, wherein the transition medium and the mold cap have approximately
14 the same coefficient of thermal expansion so as to reduce the thermal stress on the die
15 during thermal cycling.

Sub 2
a 49. (New) An integrated circuit package comprising:
1 an integrated circuit die having a front side, a back side, and a first
2 thickness between the front and back sides, wherein bonding pads are formed on the front
3 side;
4 a metallized polymer layer having a first side and a second side, wherein
5 the bonding pads are electrically coupled to features of the metallized polymer layer; and
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1 60. (New) The integrated circuit package of claim 49 wherein the
2 transition medium has a coefficient of thermal expansion between approximately
3 $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$.

1 61. (New) The integrated circuit package of claim 49 further
2 comprising:

3 solder balls, below the metallized polymer layer and integrated circuit die,
4 electrically coupled to the bonding pads.